

A2
essentially of silicon, oxygen, carbon and hydrogen and incorporating carbon therein and having a dielectric constant of less than about 3.5.

IN THE SPECIFICATION:

Please amend the specification as set forth below.

On page 14, please amend the paragraph beginning on line 8 and ending on line 14 as indicated by the clean version below:

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As shown in Figure 15, a second metal or metal 2 layer 31 is then deposited over the low k material 16" and into the contacts 17". In accordance with current circuit density, the contact 17" is difficult to fill with standard physical vapor deposition (PVD) techniques. Accordingly, the second metal layer 31 is preferably deposited by a hot metal process, such as by deposition of aluminum at greater than about 550°C. As with the dual damascene process described above, the metal deposition advantageously serves as an anneal to further lower the dielectric constant of the low k material 16".

IN THE DRAWINGS:

The Examiner has objected to the drawings as failing to comply with 37 C.F.R. 1.89(p)(4) because reference character "30" has been used to designate both the second metal layer (Fig. 15) and the gate electrode (Fig. 16). Accordingly, attached hereto are drawings in which reference character "30" in Figure 15 has been replaced with reference character "31". In addition, the specification has also been amended accordingly.

REMARKS

Claims 1-10 are pending in this application. Reconsideration is respectfully requested in view of the following remarks.

Claim Rejections under 35 U.S.C. §102

Anticipation by Yau et al.

The Examiner has rejected Claims 1-7 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,072,227 to Yau et al. ("Yau").

Amended Claim 1 recites "a *unitary* layer of insulating material *directly contacting and formed between* conductive elements in an integrated circuit...." Claims 2-4 are dependent on